Refine Search

Search Results -

Terms	Documents
L2 or L4	54

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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

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Search History

DATE: Monday, September 27, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
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L5	l2 or L4	54	L5
L4	L3 same (compar$3 near10 monitor$3)	36	L4
L3	generat$3 same trigger same output same condition	11207	L3
L2	compar$3 same (trigger adj1 condition) same bus	20	L2
L1	compar$3 near5 (trigger adj1 condition) near10 bus	2	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
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Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text Clear Interrupt

Search History

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L4	L3 same (compar$3 near10 monitor$3)	36	L4
L3	generat$3 same trigger same output same condition	11207	L3
L2	compar$3 same (trigger adj1 condition) same bus	20	L2
L1	compar$3 near5 (trigger adj1 condition) near10 bus	2	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
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Database:
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- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L7

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, September 27, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name results set
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L5	l2 or L4	54	L5
L4	L3 same (compar$3 near10 monitor$3)	36	L4
L3	generat$3 same trigger same output same condition	11207	L3
L2	compar$3 same (trigger adj1 condition) same bus	20	L2
L1	compar$3 near5 (trigger adj1 condition) near10 bus	2	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L5 and L7	9

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L8

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, September 27, 2004 Printable Copy Create Case

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L5	l2 or L4	54	L5
L4	L3 same (compar$3 near10 monitor$3)	36	L4
L3	generat$3 same trigger same output same condition	11207	L3
L2	compar$3 same (trigger adj1 condition) same bus	20	L2
L1	compar$3 near5 (trigger adj1 condition) near10 bus	2	L1

END OF SEARCH HISTORY

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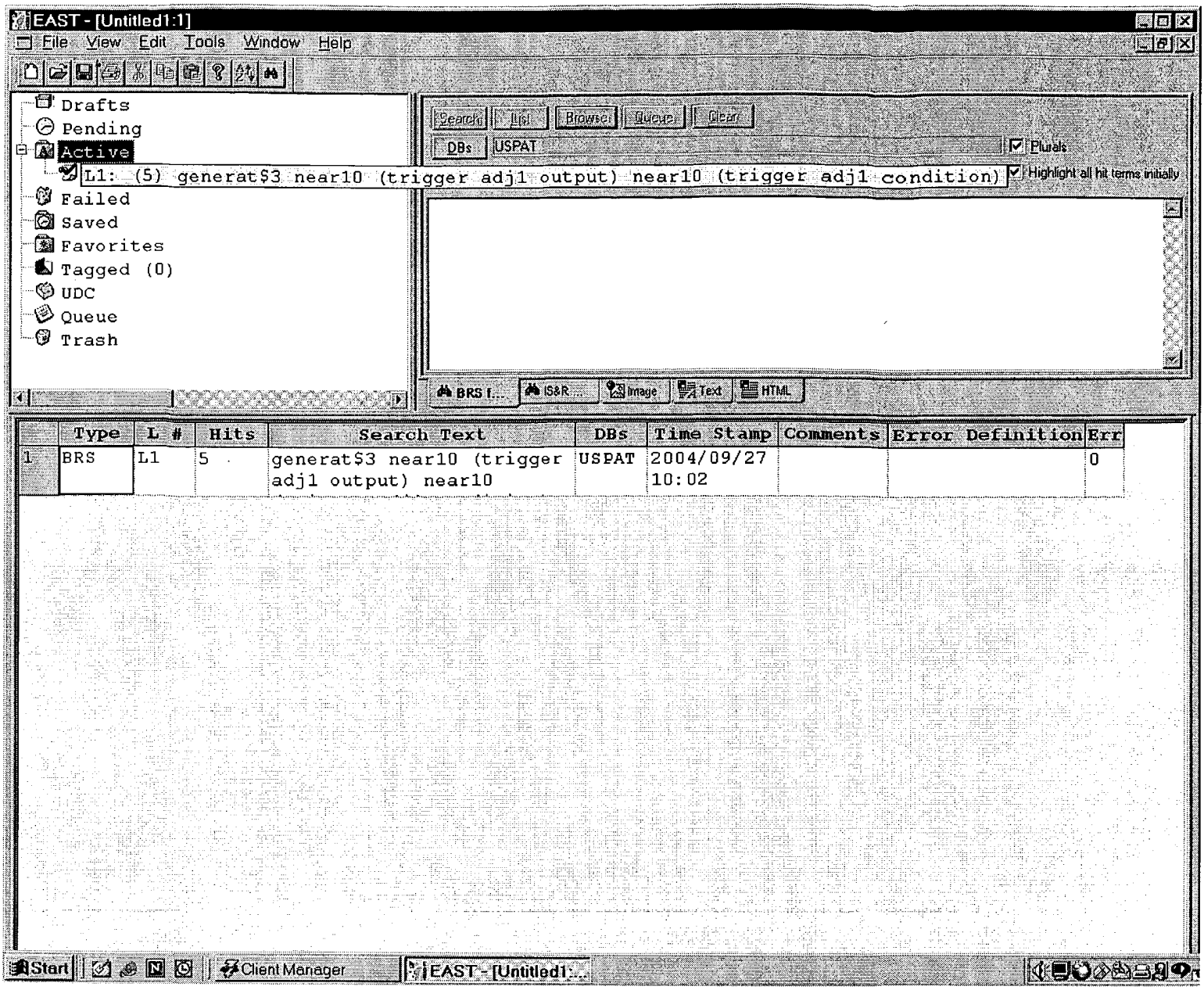
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File View Edit Tools Window Help
Drafts
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Failed
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Search Text
DBs
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Client Manager
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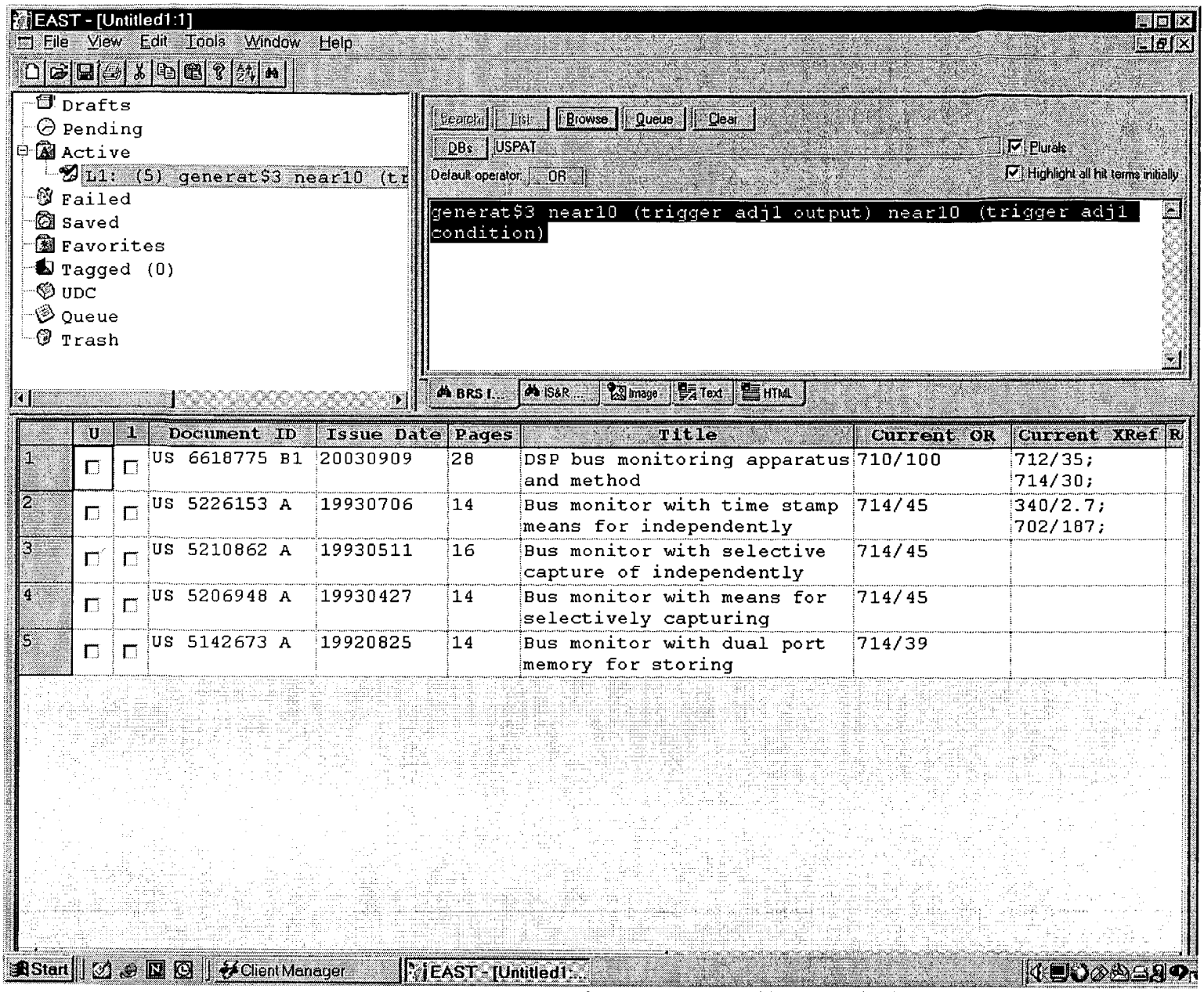

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6618775 B1	20030909	28	DSP bus monitoring apparatus and method	710/100	712/35; 714/30;	
2	☐	☐	US 5226153 A	19930706	14	Bus monitor with time stamp means for independently	714/45	340/2.7; 702/187;	
3	☐	☐	US 5210862 A	19930511	16	Bus monitor with selective capture of independently	714/45		
4	☐	☐	US 5206948 A	19930427	14	Bus monitor with means for selectively capturing	714/45		
5	☐	☐	US 5142673 A	19920825	14	Bus monitor with dual port memory for storing	714/39		

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generat* and trigger and condition and compar* Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Streamer current in a three-electrode system**
Akyuz, M.; Gao, L.; Cooray, V.; Larsson, A.;
Dielectrics and Electrical Insulation, IEEE Transactions on [see also Electrical Insulation, IEEE Transactions on] , Volume: 8 , Issue: 4 , Aug. 2001
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[Abstract] [PDF Full-Text (728 KB)] **IEEE JNL**

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2 **Charge carrier avalanche multiplication in high-voltage diodes trigg by ionizing radiation**
Soelkner, G.; Voss, P.; Kaindl, W.; Wachutka, G.; Maier, K.H.; Becker, H.-W.
Nuclear Science, IEEE Transactions on , Volume: 47 , Issue: 6 , Dec. 2000
Pages:2365 - 2372

[Abstract] [PDF Full-Text (201 KB)] **IEEE JNL**

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3 **The breakdown fields and risetimes of select gases under the condi of fast charging (/spl sim/ 20 ns and less) and high pressures (20-10 atmospheres)**
Carboni, V.; Lackner, H.; Giri, D.; Lehr, J.;
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[Abstract] [PDF Full-Text (487 KB)] **IEEE CNF**

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4 **The influence of electron density on the formation of streamers in electrical discharges triggered with ultrashort laser pulses**
La Fontaine, B.; Vidal, F.; Comtois, D.; Ching-Yuan Chien; Desparois, A.; Joh T.W.; Kieffer, J.-C.; Mercure, H.P.; Pepin, H.; Rizk, F.A.M.;

Plasma Science, IEEE Transactions on , Volume: 27 , Issue: 3 , June 1999
Pages:688 - 700

[Abstract] [PDF Full-Text (248 KB)] **IEEE JNL**

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5 **Analysis of a passive superconducting fault current limiter**
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Applied Superconductivity, IEEE Transactions on , Volume: 8 , Issue: 1 , Marc
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Pages:20 - 25

[Abstract] [PDF Full-Text (188 KB)] **IEEE JNL**

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6 **Voltage pulse forming dynamics in a transmission line section empl photoconductive charging and discharging**
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[Abstract] [PDF Full-Text (504 KB)] **IEEE JNL**

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7 **Dynamics of fibrin clot lysis under flow conditions by erythrocyte-li tPA**
Goel, M.S.; Murciano, J.-C.; Medinilla, S.; Yamamoto, A.; Cines, D.B.; Muzyk V.R.; Diamond, S.L.;
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Pages:520 vol.1

[Abstract] [PDF Full-Text (163 KB)] **IEEE CNF**

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8 **The Atlas load protection switch**
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Pulsed Power Conference, 1999. Digest of Technical Papers. 12th IEEE International , Volume: 2 , 27-30 June 1999
Pages:941 - 944 vol.2

[Abstract] [PDF Full-Text (420 KB)] **IEEE CNF**

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The Atlas load protection switch

Davis, H.A. Ballard, E.O. Dorr, G. Martinez, M. Gribble, R.F. Nielsen, K.E. Pierce, D. Parsons, W.M.
Los Alamos Nat. Lab., NM, USA;

This paper appears in: **Pulsed Power Conference, 1999. Digest of Technical Papers. 12th IEEE International**

Meeting Date: 06/27/1999 - 06/30/1999
Publication Date: 27-30 June 1999
Location: Monterey, CA USA
On page(s): 941 - 944 vol.2
Volume: 2
Reference Cited: 6
Number of Pages: 2 vol. 1529
Inspec Accession Number: 6537420

Abstract:
Atlas is a high-energy pulsed-power facility under development to study materials properties and hydrodynamics experiments under extreme **conditions**. Atlas will implode heavy liner loads (m~45 gm) with a peak current of 27-32 MA delivered in 4 μs, and is energized by 96, 240 kV Marx **generators** storing a total of 23 MJ. A key design requirement for Atlas is obtaining useful data for 95% of all loads installed on the

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Print Format

machine. Materials response calculations show current from a prefire can damage the load requiring expensive and time consuming replacement. Therefore, we have incorporated a set of fast-acting mechanical switches in the Atlas design to reduce the probability of a prefire damaging the load. These switches, referred to as the load protection switches, short the load through a very low inductance path during system charge. Once the capacitors have reached full charge, the switches open on a time scale short **compared** to the bank charge time, allowing current to flow to the load when the **trigger** pulse is applied. The time window of vulnerability for load damage is thus substantially reduced. The design of the load protection switches and test results are presented

Index Terms:

protection pulse **generators** pulsed power supplies pulsed power switches 23 MJ 240 kV 27 to 32 MA 4 mus 45 g Atlas load protection switch Marx **generators** fast-acting mechanical switches heavy liner loads implosion high-energy pulsed-power facility hydrodynamics experiments materials properties materials response calculations prefire current **trigger** pulse very low inductance path

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(12) **United States Patent**
Davis

(10) **Patent No.: US 6,618,775 B1**
(45) **Date of Patent: Sep. 9, 2003**

(54) **DSP BUS MONITORING APPARATUS AND METHOD**

(75) Inventor: **Henry A. Davis**, Soquel, CA (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/638,461

(22) Filed: **Aug. 14, 2000**

Related U.S. Application Data

(63) Continuation of application No. 09/026,734, filed on Feb. 20, 1998, now abandoned.
(60) Provisional application No. 60/055,815, filed on Aug. 15, 1997.

(51) Int. Cl.[7] G06F 11/30; G05F 13/00
(52) U.S. Cl. 710/100; 714/30; 714/45; 712/35
(58) Field of Search 714/47, 30, 25, 714/40, 45, 39; 710/52, 100, 305; 712/33, 35; 717/128, 129; 713/502; 345/10, 700

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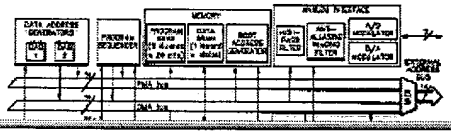
(List continued on next page.)

Primary Examiner—Gopal C. Ray
(74) *Attorney, Agent, or Firm*—Gazdzinski & Associates

(57) **ABSTRACT**

A bus monitor is provided as a tool for developing, debugging and testing a system having an embedded processor. The bus monitor resides within the same chip or module as the processor, which allows connection to internal processor buses not accessible from external contacts. The monitor uses a separate circular buffer to continuously store, in real-time, data traces from each of one or more internal processor buses. Upon the occurrence of a trigger condition, storage stops and a trace is preserved. Trigger conditions can depend on events occurring on multiple buses and are downloaded via an interface from an external device. Data traces are uploaded via the interface to an external device for evaluation of processor operation.

13 Claims, 18 Drawing Sheets



US005142673A

United States Patent [19]

De Angelis et al.

[11] Patent Number: 5,142,673

[45] Date of Patent: Aug. 25, 1992

[54] BUS MONITOR WITH DUAL PORT MEMORY FOR STORING SELECTABLE TRIGGER PATTERNS

[75] Inventors: Douglas J. De Angelis, Woburn; Henry W. J. Maddox, Franklin; Arthur Peters, Sudbury; Donald J. Rathbun, Methuen; William L. Saltmarsh, Brockton, all of Mass.

[73] Assignee: Bull HN Information Systems Inc., Billerica, Mass.

[21] Appl. No.: 456,664

[22] Filed: Dec. 22, 1989

[51] Int. Cl.[5] G06F 11/34

[52] U.S. Cl. 395/575; 364/267; 364/267.2

[58] Field of Search ..... 371/19, 15.1, 16.1; 364/200 MS File, 900 MS File

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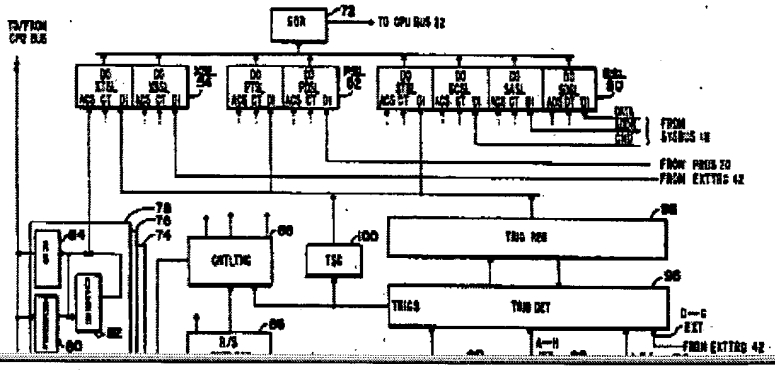
5,001,714	3/1991	Stark et al.	371/26

Primary Examiner—Jerry Smith
Assistant Examiner—Phung Mychung
Attorney, Agent, or Firm—Gary D. Clapp; John S. Solakian

[57] ABSTRACT

A monitor for selectively detecting and recording conditions at selected points within a system includes a trigger memory for storing patterns of trigger signals, wherein each pattern of trigger signals corresponds to a selected condition to be detected on first points of the system. The trigger memory includes a first port having a read address input connected from the first points and a data output connected to trigger output logic for providing patterns of trigger signals corresponding to the conditions to be detected. Each pattern of trigger signals is stored in the trigger memory location whose address corresponds to a pattern of signals from the first points representing the corresponding condition to be detected. The trigger memory is a dual port memory having a second port with a write address input and a data input for receiving trigger patterns to be stored therein. The method for generating the trigger patterns includes generating a first trigger pattern map and, from the first map, a second trigger pattern map to be written into a trigger memory which includes a plurality of submemories, wherein each submemory stores a portion of the trigger patterns.

6 Claims, 4 Drawing Sheets



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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 20030120980 A1

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L8: Entry 1 of 9 File: PGPB Jun 26, 2003

PGPUB-DOCUMENT-NUMBER: 20030120980
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030120980 A1

TITLE: System trace unit

PUBLICATION-DATE: June 26, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Harris, Jeremy G.	Buckinghamshire		GB	

US-CL-CURRENT: 714/45

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6618775 B1

L8: Entry 2 of 9 File: USPT Sep 9, 2003

US-PAT-NO: 6618775
DOCUMENT-IDENTIFIER: US 6618775 B1
** See image for Certificate of Correction **

TITLE: DSP bus monitoring apparatus and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 3. Document ID: US 6378092 B1

L8: Entry 3 of 9 File: USPT Apr 23, 2002

US-PAT-NO: 6378092
DOCUMENT-IDENTIFIER: US 6378092 B1

TITLE: Integrated circuit testing

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 4. Document ID: US 5964893 A

L8: Entry 4 of 9 File: USPT Oct 12, 1999

US-PAT-NO: 5964893
DOCUMENT-IDENTIFIER: US 5964893 A

TITLE: Data processing system for performing a trace function and method therefor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 5. Document ID: US 5581745 A

L8: Entry 5 of 9 File: USPT Dec 3, 1996

US-PAT-NO: 5581745
DOCUMENT-IDENTIFIER: US 5581745 A

TITLE: Apparatus for suspending the bus cycle of a microprocessor by inserting wait states

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 6. Document ID: US 5226153 A

L8: Entry 6 of 9 File: USPT Jul 6, 1993

US-PAT-NO: 5226153
DOCUMENT-IDENTIFIER: US 5226153 A

TITLE: Bus monitor with time stamp means for independently capturing and correlating events

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 7. Document ID: US 5210862 A

L8: Entry 7 of 9 File: USPT May 11, 1993

US-PAT-NO: 5210862
DOCUMENT-IDENTIFIER: US 5210862 A

TITLE: Bus monitor with selective capture of independently occuring events from multiple sources

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 8. Document ID: US 5206948 A

L8: Entry 8 of 9 File: USPT Apr 27, 1993

US-PAT-NO: 5206948
DOCUMENT-IDENTIFIER: US 5206948 A

TITLE: Bus monitor with means for selectively capturing trigger conditions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 9. Document ID: US 5142673 A

L8: Entry 9 of 9 File: USPT Aug 25, 1992

US-PAT-NO: 5142673
DOCUMENT-IDENTIFIER: US 5142673 A

TITLE: Bus monitor with dual port memory for storing selectable trigger patterns

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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Terms	Documents
L5 and L7	9

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L8: Entry 2 of 9 File: USPT Sep 9, 2003

US-PAT-NO: 6618775
DOCUMENT-IDENTIFIER: US 6618775 B1
**** See image for Certificate of Correction ****

TITLE: DSP bus monitoring apparatus and method

DATE-ISSUED: September 9, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Davis; Henry A.	Soquel	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Technology, Inc.	Boise	ID			02

APPL-NO: 09/ 638461 [PALM]
DATE FILED: August 14, 2000

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATION This application is a continuation of U.S. patent application Ser. No. 09/026,734 filed Feb. 20, 1998 entitled "DSP Bus Monitoring Apparatus And Method", abandoned. Pursuant to 35 U.S.C. .sctn.119(e), this application claims the priority benefit of provisional application No. 60/055,815 filed Aug. 15, 1997.

INT-CL: [07] G06 F 11/30, G06 F 13/00

US-CL-ISSUED: 710/100; 714/30, 714/45, 712/35
US-CL-CURRENT: 710/100; 712/35, 714/30, 714/45

FIELD-OF-SEARCH: 714/47, 714/30, 714/25, 714/40, 714/45, 714/39, 710/52, 710/100, 710/305, 712/33, 712/35, 717/128, 717/129, 713/502, 345/10, 345/700

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5142673	August 1992	DeAngelis et al.	395/575
☐	5210862	May 1993	DeAngelis et al.	395/575
☐	5313618	May 1994	Pawloski	395/500.49

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☐	5325368	June 1994	James et al.	714/727
☐	5329471	July 1994	Swoboda et al.	395/500.44
☐	5355369	October 1994	Greenberger et al.	714/724
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ATTY-AGENT-FIRM: Gazdzinski & Associates

ABSTRACT:

A bus monitor is provided as a tool for developing, debugging and testing a system having an embedded processor. The bus monitor resides within the same chip or module as the processor, which allows connection to internal processor buses not accessible from external contacts. The monitor uses a separate circular buffer to continuously store, in real-time, data traces from each of one or more internal processor buses. Upon the occurrence of a trigger condition, storage stops and a trace is preserved. Trigger conditions can depend on events occurring on multiple buses and are downloaded via an interface from an external device. Data traces are uploaded via the interface to an external device for evaluation of processor operation.

13 Claims, 45 Drawing figures

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